At **650**, a polysilicon layer is deposited on the first dielectric layer. In one implementation, the polysilicon is deposited by a method such as decomposition of silane (SiH_4). The polysilicon may be doped by introducing the impurity during the deposition process or in a separate doping process. In the n-channel MOSFET implementation, the polysilicon may be heavily doped with Phosphorus or Arsenic (N+) at a concentration of approximately 1.0E17 cm^{-3} to 1.0E20 cm^{-3}. In the p-channel MOSFET implementation, the polysilicon may be heavily doped with Boron (P+). At **655**, a fourth photo-resist may be deposited and patterned by any well-known lithography process to define the gate regions. Referring now to FIG. **6**C, the portions of the first dielectric layer, polysilicon layer and second dielectric layer exposed by the fourth patterned photo-resist may be removed by any well-known etching process, at **660**. At **665**, the fourth patterned photo-resist layer may be removed utilizing an appropriate resist stripper or resist ashing process.

At **670**, a second dielectric layer is on the wafer. The second dielectric layer completes the gate insulator regions disposed about the gate regions. The second dielectric layer may be formed by any well-known oxidation processes. At **675**, a fifth photo-resist may be deposited and patterned by any well-known lithography process to define a plurality of source-body contact openings between the gate regions. At **680**, the portions of the second dielectric layer exposed by the fifth patterned photo-resist may be removed by any well-known etching process. At **682**, the fifth patterned photo-resist layer may be removed utilizing an appropriate resist stripper or resist ashing process.

Referring now to FIG. **6**D, a source-body metal layer is deposited on the surface of the wafer, at **684**. The source-body metal layer may be deposited such that the first second and third plurality of well regions and a fourth portion of the first semiconductor layer disposed between the second plurality of well regions are electrically coupled to each other. In one implementation, the source-body metal layer is deposited by any well-known method such as sputtering. The source-body metal layer forms a contact with the body and source regions left exposed by the patterned second dielectric layer. The source-body metal layer is isolated from the gate region by the patterned first second and third dielectric layers. The source-body metal layer also forms a Schottky barrier at the interface of the epitaxial deposited layer disposed between the first, second and third well regions. The source-body metal layer is then patterned utilizing a photo-resist mask and selective etching method as needed, at **686**. At **688**, fabrication continues with various other processes. The various processes typically include etching, deposition, doping, cleaning, annealing, passivation, cleaving and/or the like.

Accordingly, embodiments of the present invention provide JFET devices provide JFET devices having reduced leakage current and/or faster switching, as compared to conventional power MOSFET devices. The JFET devices having reduced leakage current and/or faster switching characteristics may advantageously be utilized in many applications such as high-frequency DC-DC converters and the like.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

What is claimed is:

1. A field effect transistor comprising:

a semiconductor substrate having a top surface and a bottom surface, wherein the semiconductor substrate includes a drain region therein;

a trench gate region extending into the semiconductor substrate for a first predetermined depth, wherein the trench gate region is insulated from the semiconductor substrate by a gate insulator region;

a pair of source regions in the semiconductor substrate and disposed on opposite sides of the trench gate region;

a pair of body regions extending into the semiconductor substrate for a second predetermined depth and disposed on opposite sides of the trench gate region, wherein each of the body regions separates a respective source region from the drain region and the second predetermined depth is less than the first predetermined depth;

a source metal contact disposed on the top surface of the semiconductor substrate, wherein the source metal contact is in physical contact with the pair of source regions, the pair of body regions, and a portion of the drain region, wherein the source metal contact is insulated from the trench gate region by the gate insulator region; and

a drain metal contact disposed on the bottom surface of the semiconductor substrate, wherein the drain metal contact is in physical contact with the drain region;

wherein each of the body regions further includes a lightly-doped body region below a respective source region and a heavily-doped body region above the lightly-doped body region such that the heavily-doped body region is in physical contact with the source metal contact and the lightly-doped body region is not in physical contact with the source metal contact.

2. The field effect transistor of claim **1**, wherein:

the pair of source regions and the drain region are n-doped; and

the pair of body regions are p-doped.

3. The field effect transistor of claim **2**, wherein said drain region comprises:

a heavily n-doped portion and a lightly n-doped portion;

wherein the heavily n-doped portion is in physical contact with the drain metal contact and the lightly n-doped portion is in physical contact with the pair of body regions and the source metal contact.

4. The field effect transistor of claim **2**, wherein:

the lightly p-doped body region is disposed between the respective source region, the gate insulator region, and the drain region proximate the trench gate region; and

the heavily p-doped body region is disposed between the drain region, the lightly p-doped body region, the respective source region, and the source metal contact.

5. The field effect transistor of claim **1**, wherein:

the pair of source regions and the drain region are p-doped; and

the pair of body regions are n-doped.

6. The field effect transistor of claim **5**, wherein said drain region comprises:

a heavily p-doped portion and a lightly p-doped portion;

wherein the heavily p-doped portion is in physical contact with the drain metal contact and the lightly p-doped portion is in physical contact with the pair of body regions and the source metal contact.